# High Density Capacitor for Power Management Applications and its Integration in the SiP

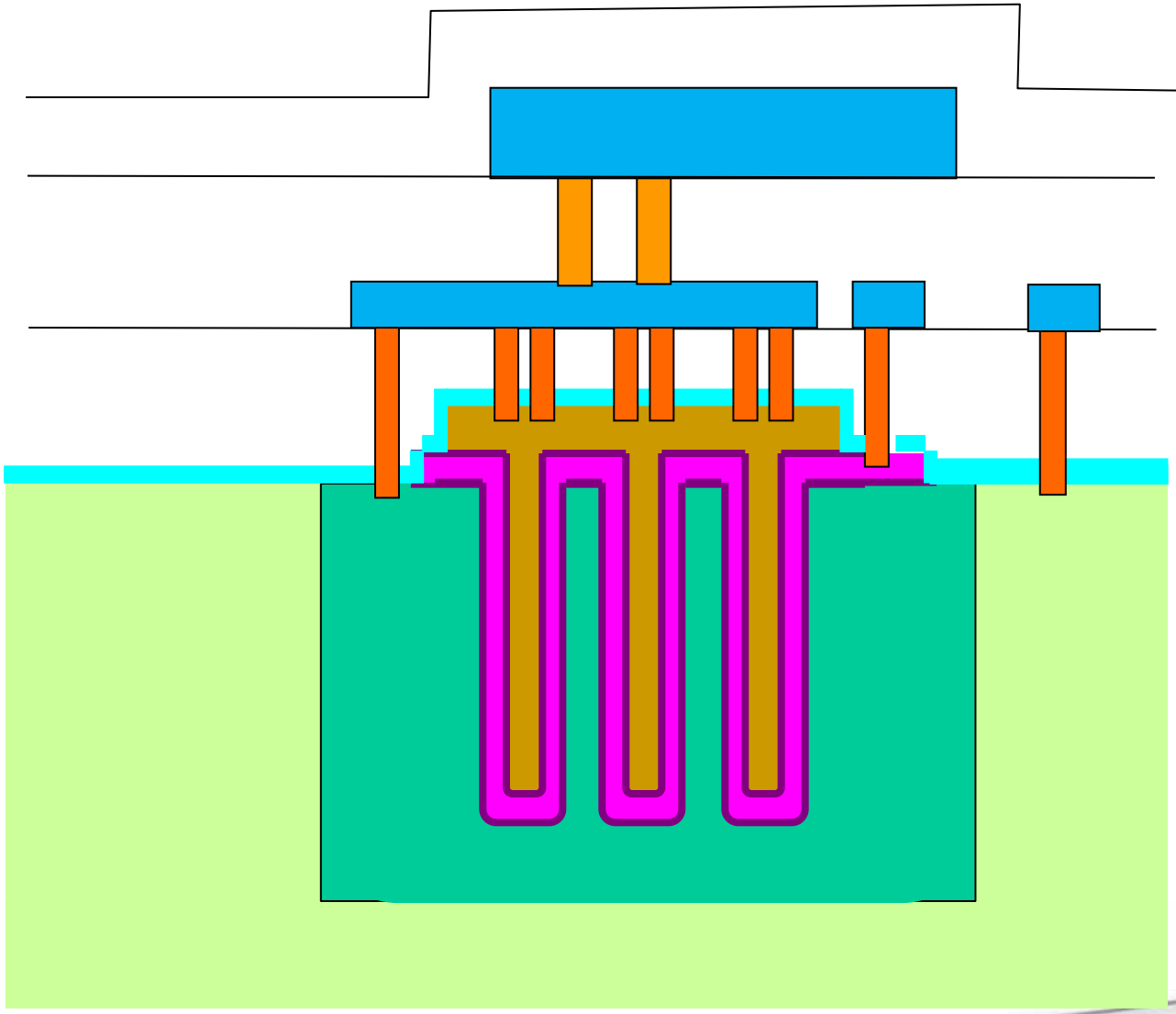
**Alexander Kalnitsky, Felix Tsui, H.L. Cheng, J.H. Yang, J.Y. Lin, Y.W. Chen, L.S. Jeng, D.N. Yaung, S.G. Wuu**

***Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan***

# Outline

- High Density Capacitor
  - Capacitance density for various operating voltages
  - AC characteristics
- Capacitor die attachment techniques
  - Surface mount (on a substrate or another die)
  - Advanced wafer to wafer attachment techniques
- Summary and conclusions

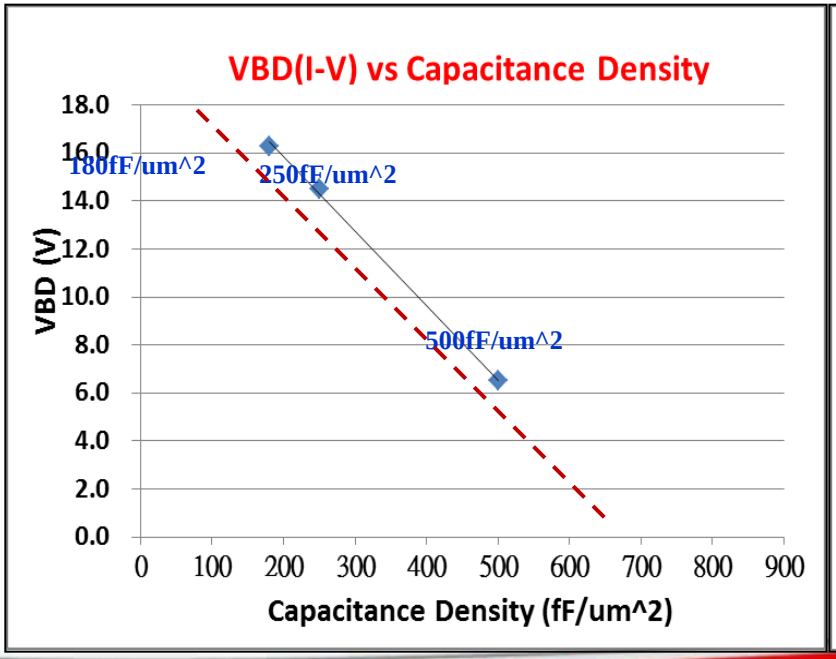
# Deep Trench Capacitor Structure

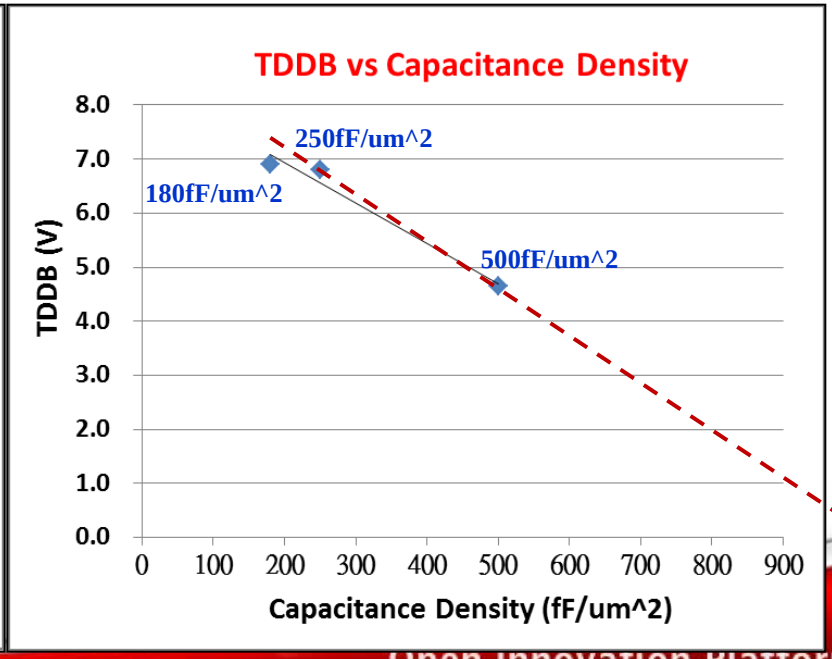


# Deep Trench Capacitor characteristics



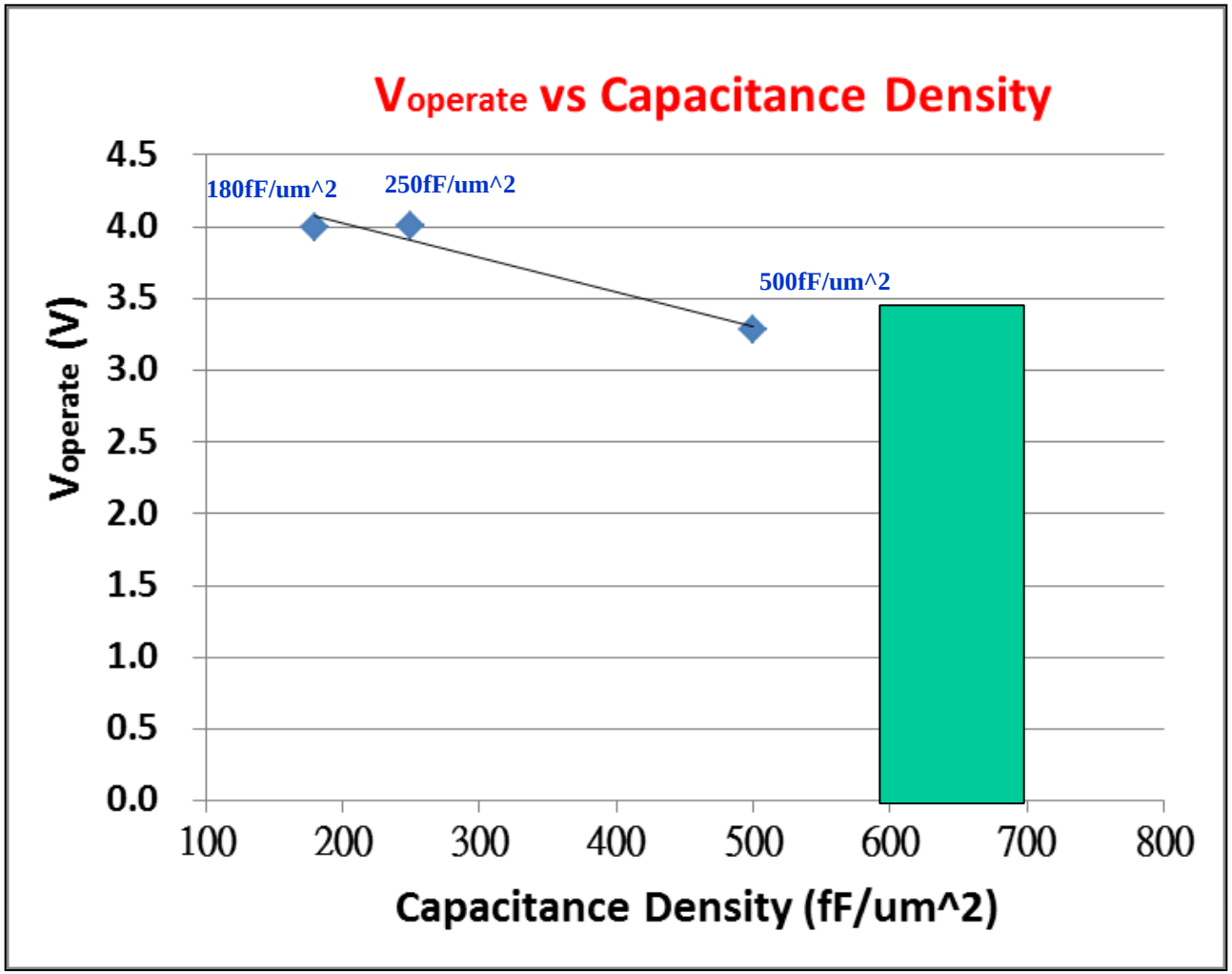
| Density, nF/mm2 | Breakdown Voltage, V | TDDB, V | Max Voltage rating, V |
|---|---|---|---|
| 180 | 16.1 | 7.0 | 4.5 |
| 250 | 14.3 | 6.8 | 4.2 |
| 500 | 6.5 | 4.5 | 3.2 |
| 600-700 | 4.0 | 3.8 | 2.5-1.2 |



# DTC Capacitor Density v.s. Vcc, TDDB, VBD

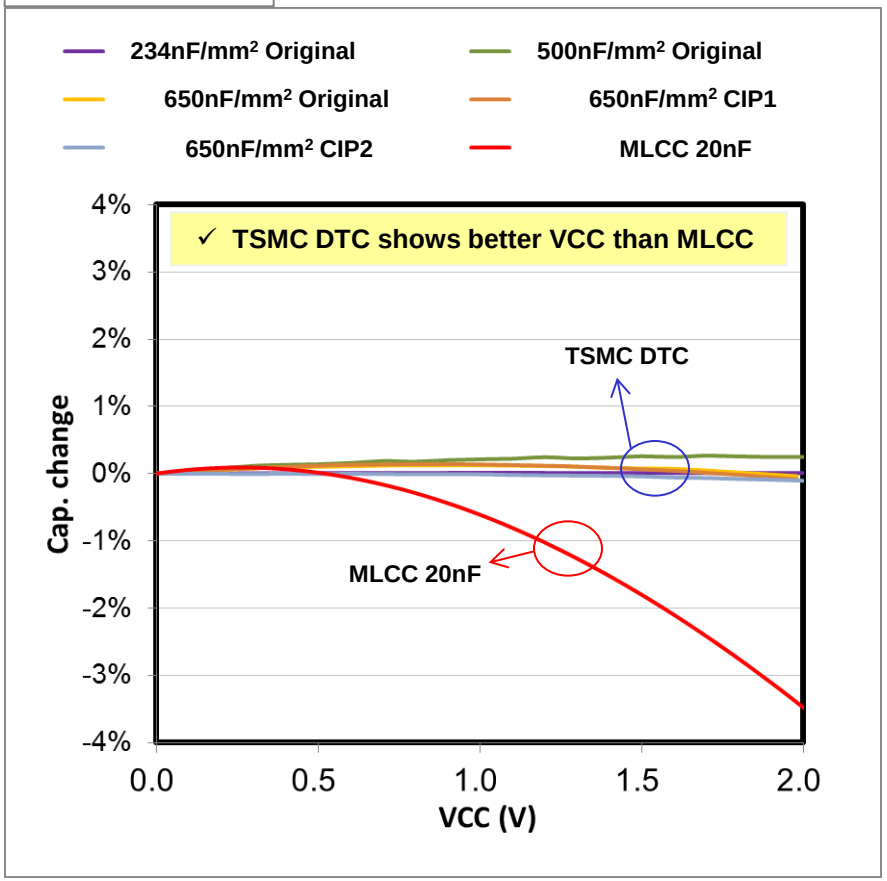


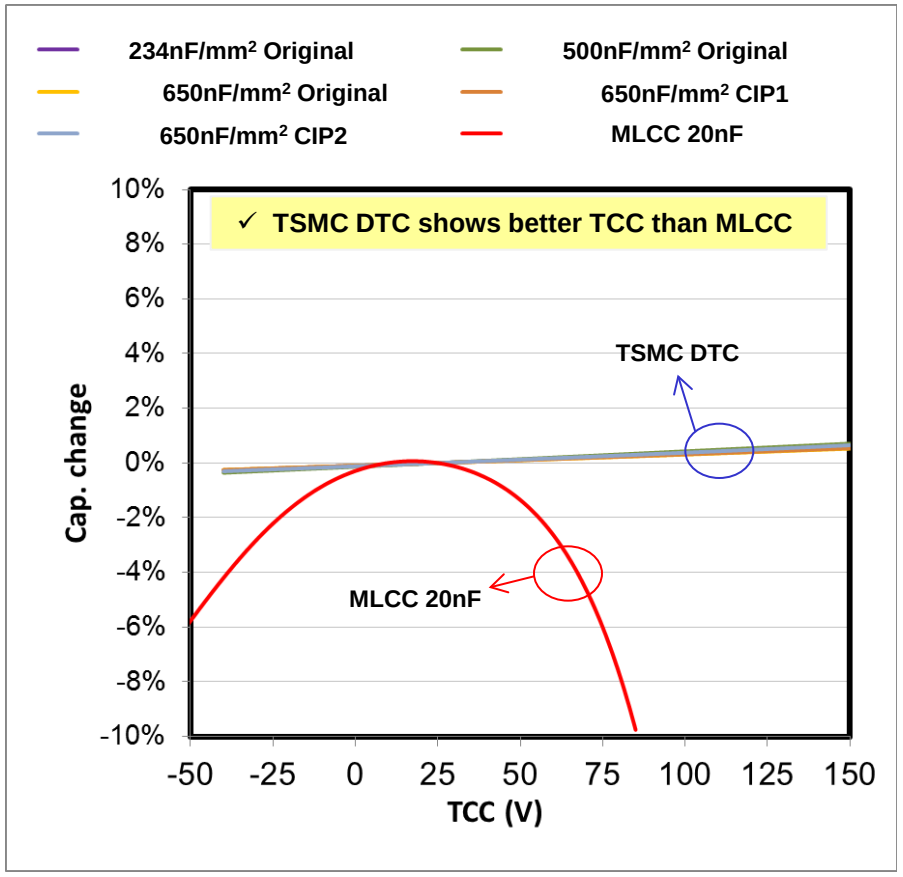


# Integrated capacitor Vcc and Tcc vs MLCC (~20nF device)



**10nF T06-RF Pattern**

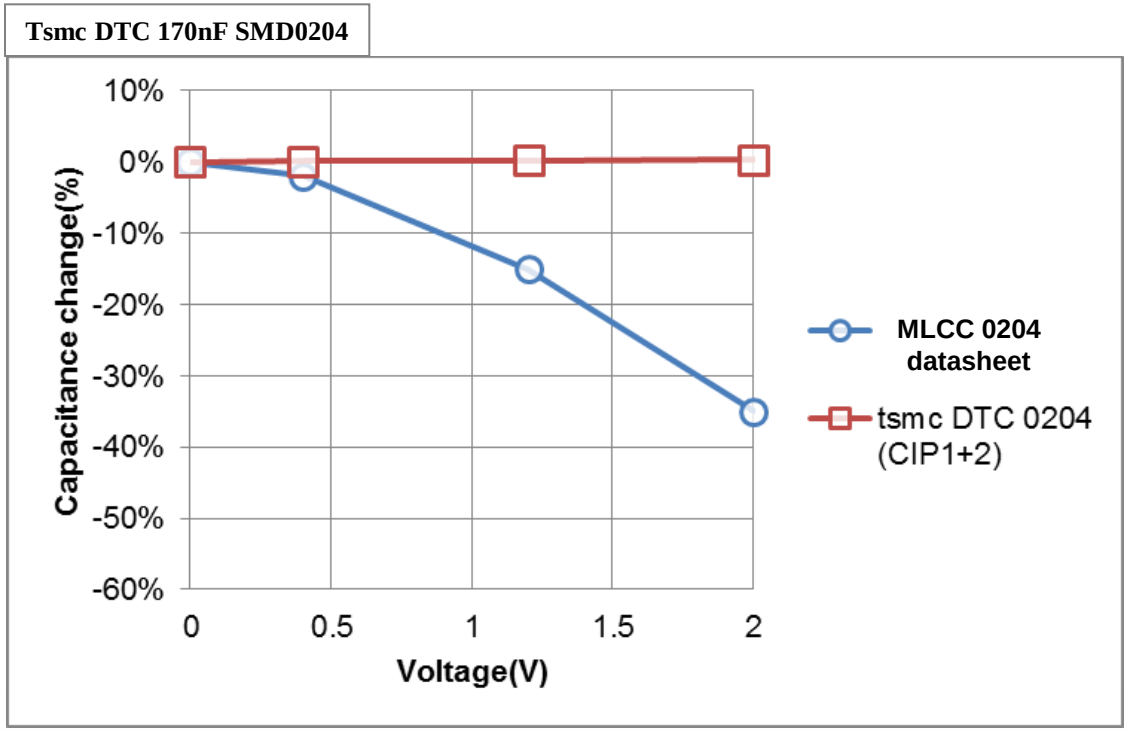


# TSMC DTC 0204(170nF) vs another vendor's MLCC SMD0204(220nF)



- **Our integrated device VCC is superior to that reported for the MLCC SMD0204**

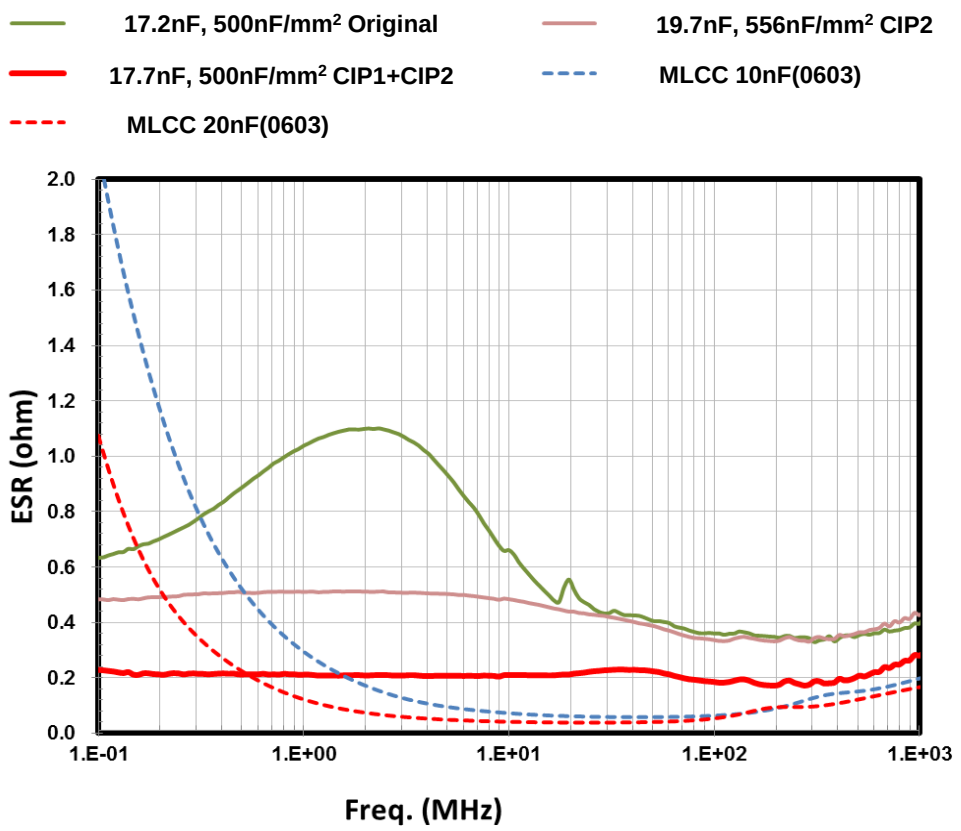


# Integrated capacitor frequency response

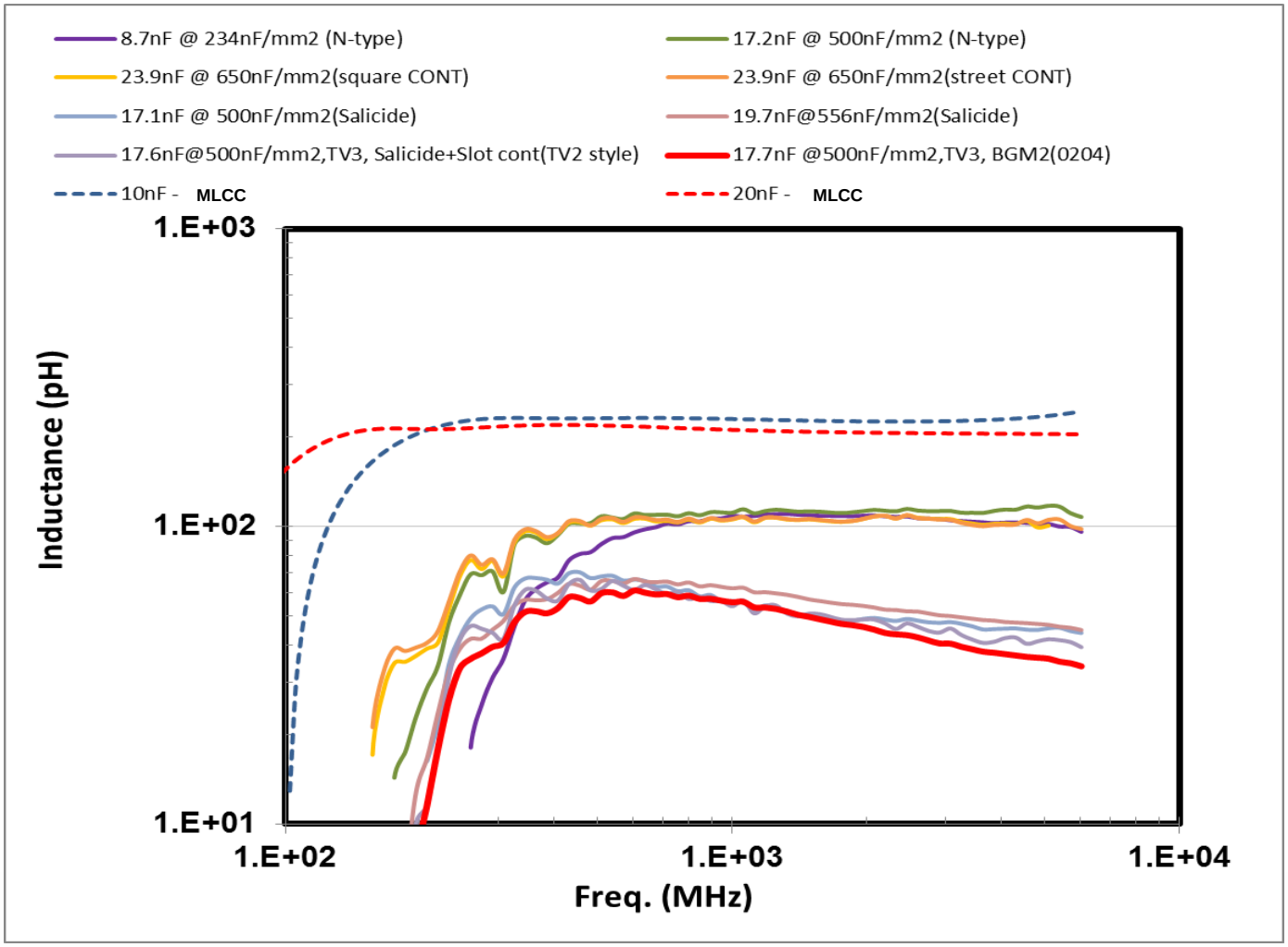


- ✓ TSMC CIP2: Reduced ESR “hump “ (low frequency to 10MHz)
- ✓ TSMC CIP1+2: Improve ESR to around 0.2ohm level

10nF T06-RF Pattern, capacitance density around 500nF/mm2



# Equivalent Series Inductance

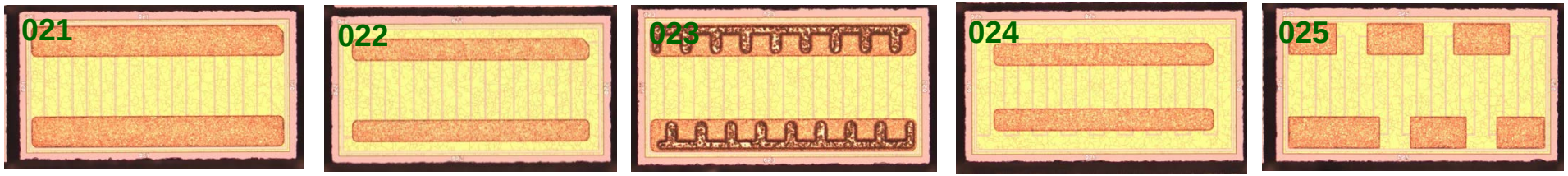


# Surface Mount Assembly

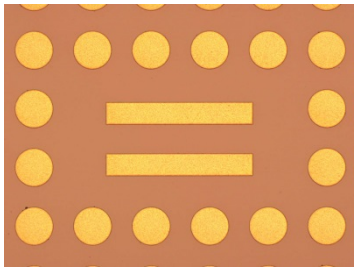
## Approach #1 solder stenciled on soldering pads



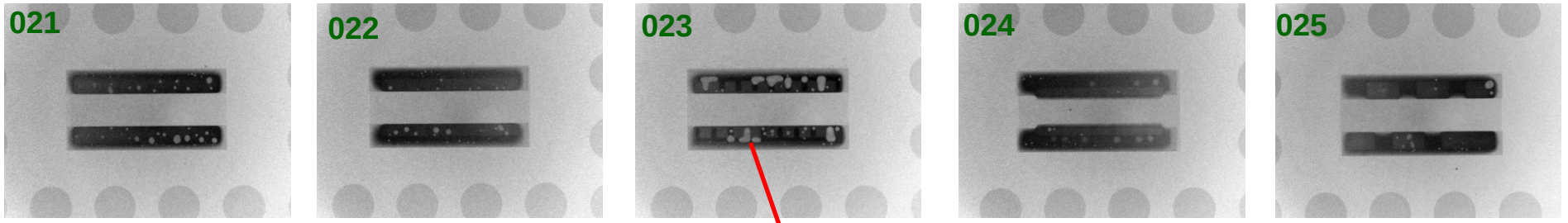
**IPD die**




**Substrate soldering pads**



**After reflow**

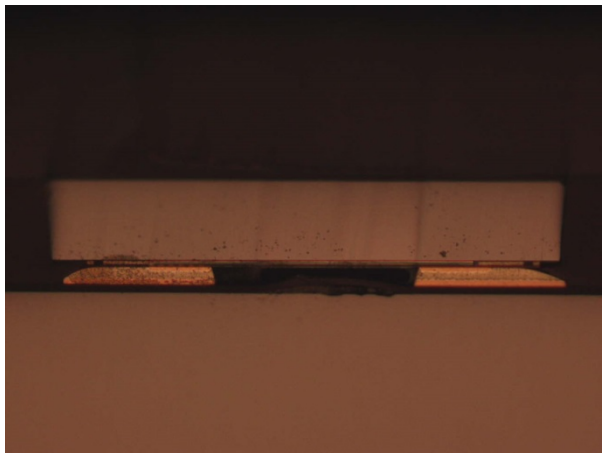


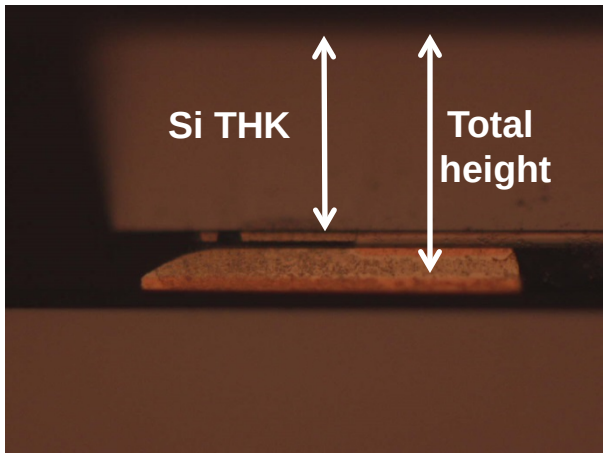

Many voids trapped

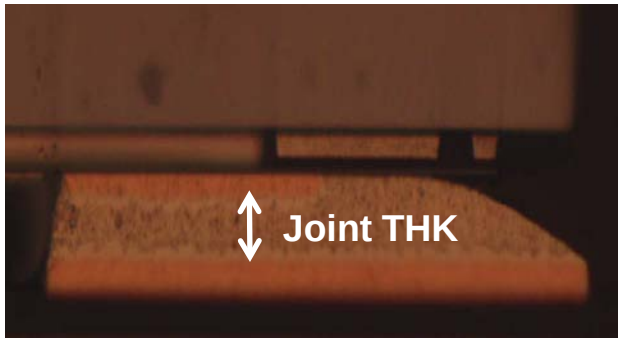
# Approach#1 solder stenciled on soldering pads



| IPD device type | 21 | 22 | 23 | 24 | 25 | AVG |
|---|---|---|---|---|---|---|
| Si THK(um) | 78.9 | 79.8 | 78.4 | 76.1 | 77.5 | 78.1 |
| Solder THK(um) | 9 | 9.4 | 12.4 | 9.7 | 13.4 | |
| Total height(um) | 100.8 | 98.5 | 102.7 | 95.7 | 100.8 | |



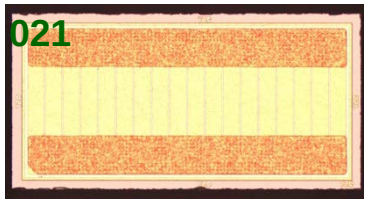


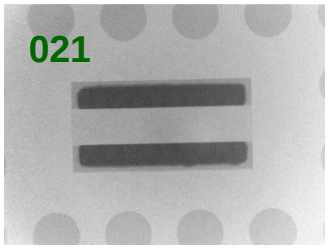
# Approach#2 solder plated on IPD die



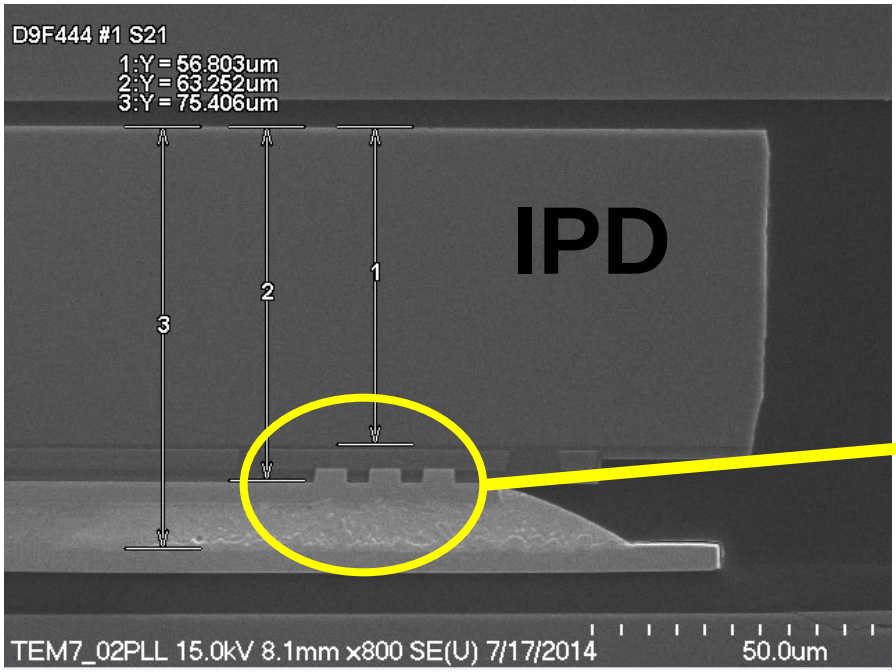
**Die front side**

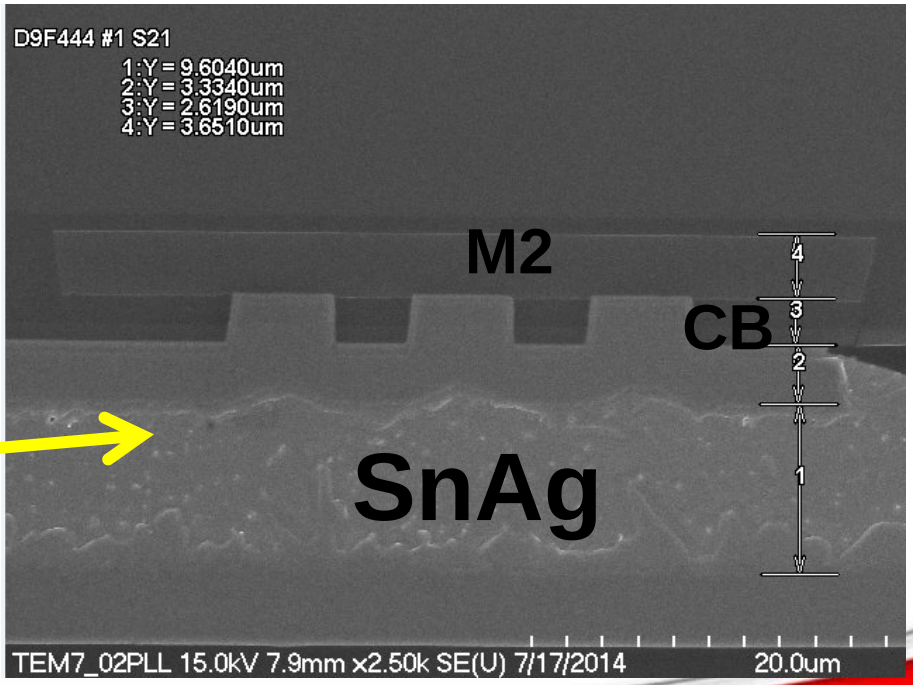



**After reflow**




| Ti/Cu/Ni/Sn Ag | In-line measures | X-SEM |
|---|---|---|
| Si THK | Avg 71.4um (69~73um) | 63.3um |
| Joint THK | N/A | 9.6um |
| Total Height | N/A | 75.4um |

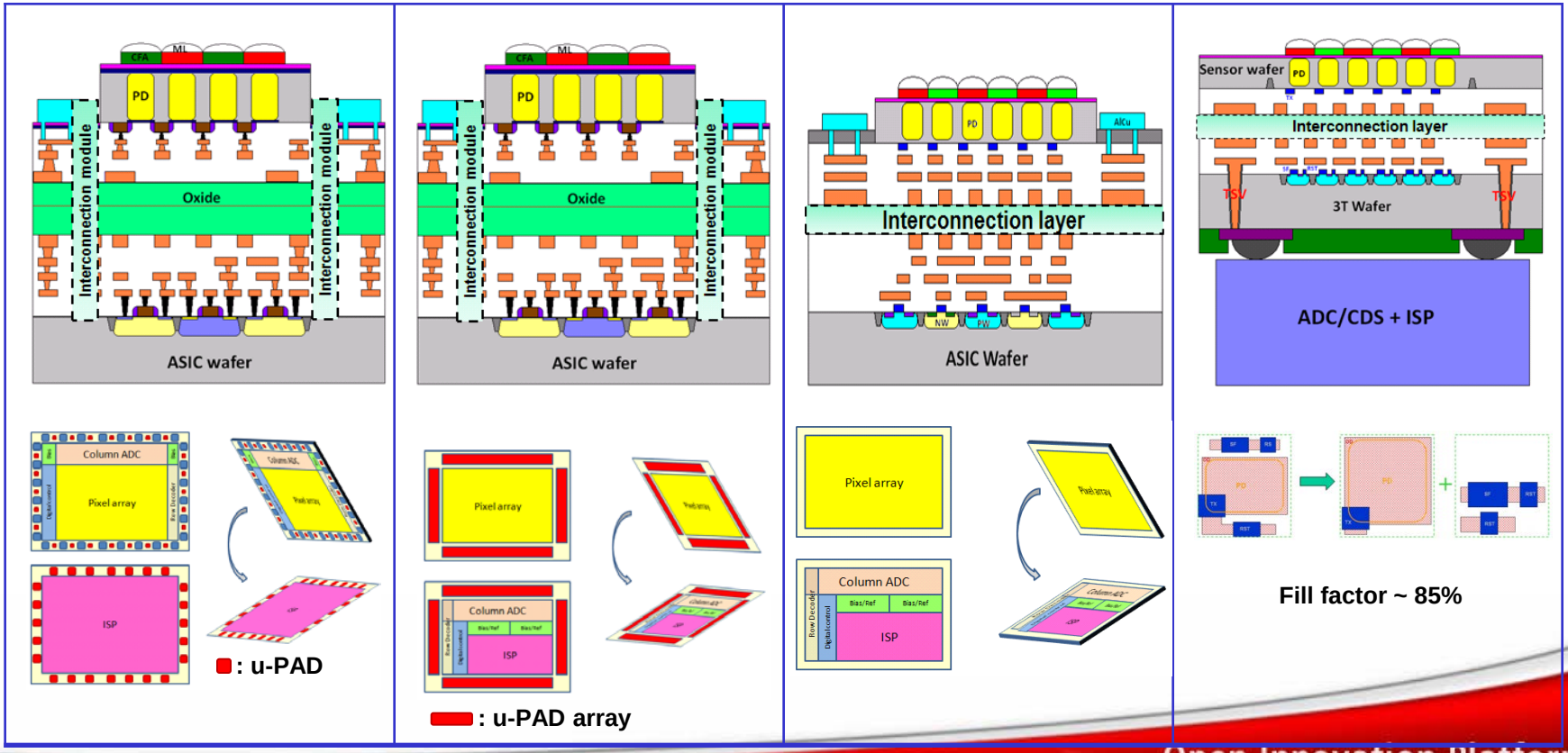


# 3D Structures (developed for BSI)

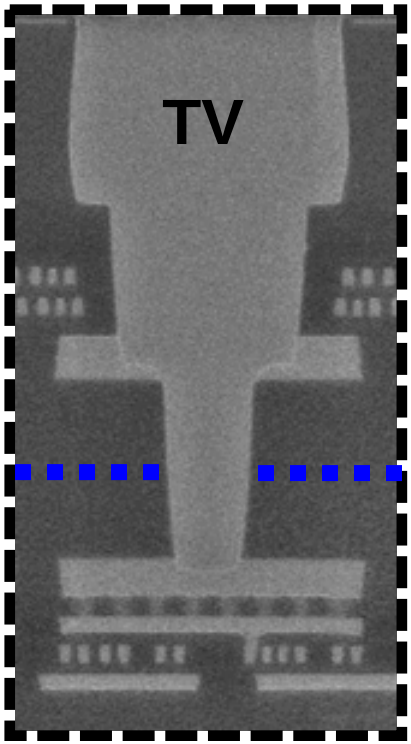


| **Phase-1** *(Chip level)* | **Phase-1 plus** *(Column level)* | **Phase-2** *(Column level)* | **Phase-3** *(Pixel level)* |
|---|---|---|---|
| u-PAD no. < 100 | u-PAD no. ~ row/column no. (k) | Inter-PAD no. ~ row/column no. (k) | Inter-PAD no. ~ pixel no. (M) |

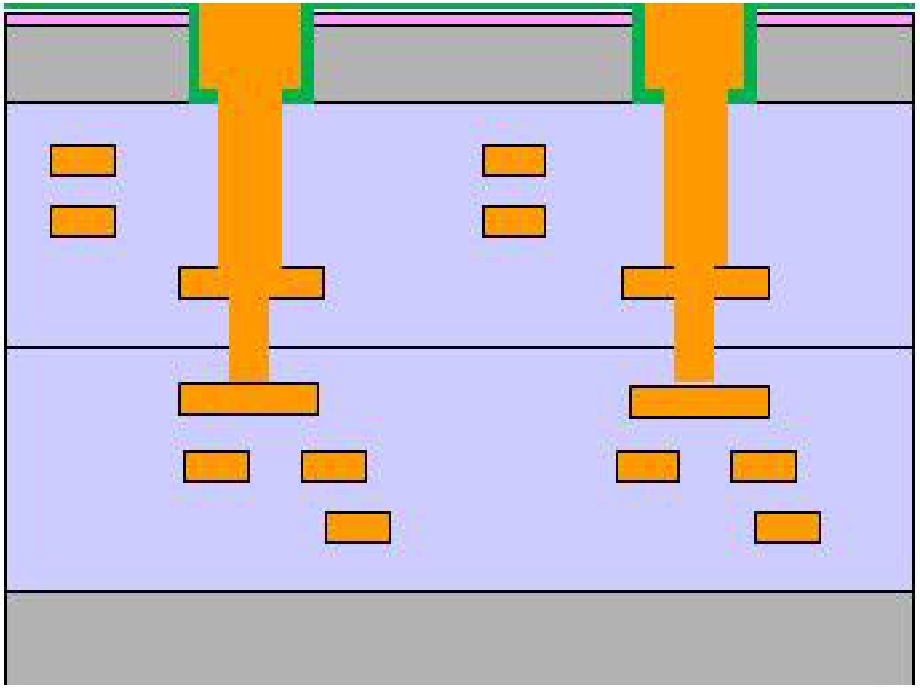


# Wafer Level Bonding

- With the improved process control, the TVs fabrication problems could be solved.



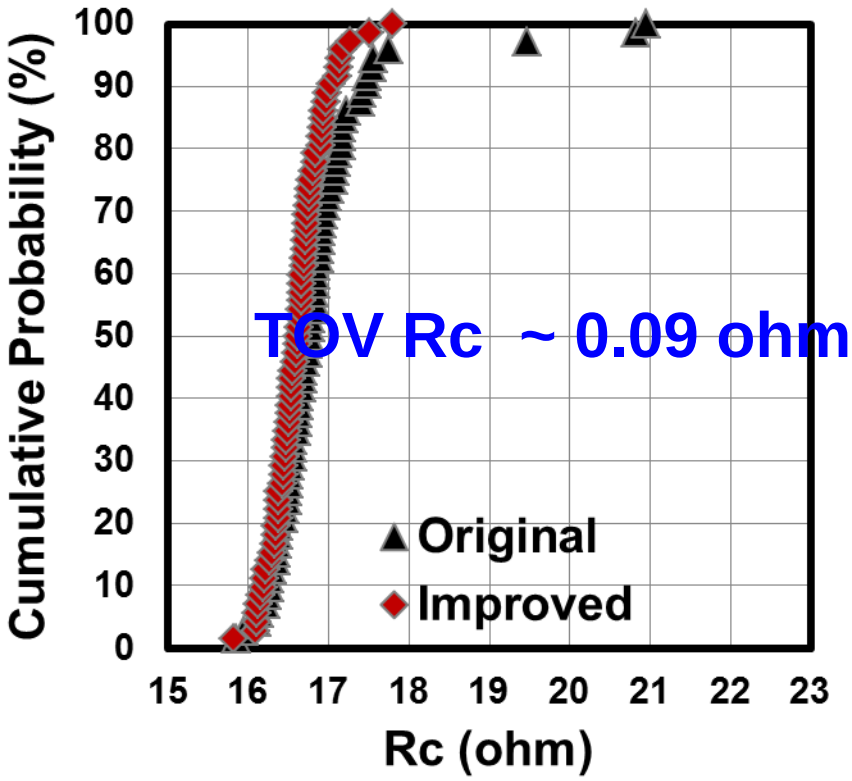

Interface



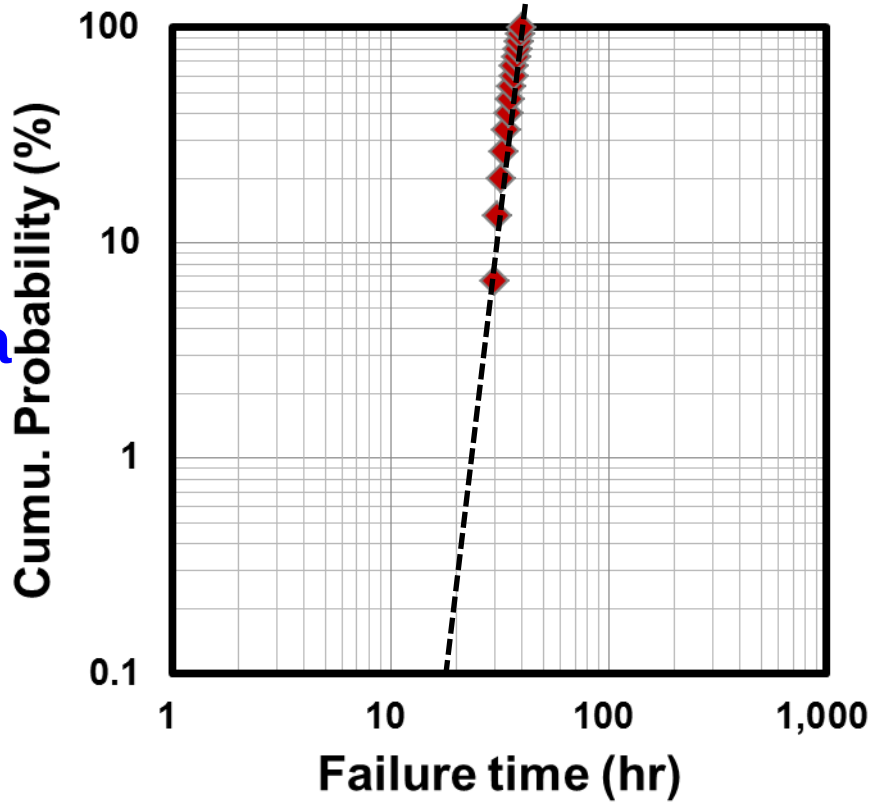
# TVs Electrical Characteristics

- TVs with a low resistance & tight distribution are achieved.
- Robust EM performance in the proposed TVs structure

## Daisy chain Rc check




## Electro Migration Test



# Summary and conclusions

- Deep trench capacitor with density up to 500nF/mm2 was demonstrated
  - Capacitance density limit for 1.2V is expected to be in the 600-700nF/mm2 range
  - ESR is comparable to commercially available caps, ESL, VCC, TCC are superior to commercially available discrete components
- Deep trench capacitors used for surface mount can achieve record thickness of ~70-100um
- TSMC developed wafer to wafer bonding processes can be used to assemble dice from different technologies (eg trench capacitor with the PMIC)